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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/737,606

12/14/2000

Pierre Leroux

8081

24738

7590

11/17/2004

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION  
INTELLECTUAL PROPERTY & STANDARDS  
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SAN JOSE, CA 95131

EXAMINER

MAGEE, THOMAS J

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/737,606	Applicant(s) LEROUX, PIERRE	
	Examiner Thomas J. Magee	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1- 5, 7, and 21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7, and 21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Cancellations***

1. Applicant's cancellation of Claim 6 in Letter of 13 July, 2004 is acknowledged.

### ***Claim Rejections – 35 U.S.C. 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to point out and distinctly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 2 recites the limitation, "an alignment target is located at each midpoint of a side of said stepper shot." There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections – 35 U.S.C. 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 – 3, 7, and 21 are rejected under 35 U.S.C. 102(e) as being as being

anticipated by Zhou (US 6,172,409 B1).

8. Regarding Claims 1 and 2, Zhou discloses a wafer for fabricating integrated circuits using a stepper, said wafer comprising:

a first region of the wafer, comprising the two chips shown in Figure 4, additional chips in the horizontal (or x axis) direction to the right and left and chips in the vertical (or y) direction (down), as part of the repetitive structure (Col. 1, lines 19 – 23) (Col. 7, line 29 through Col. 8, line 2) on the semiconductor wafer, with scribe lines (32) "along" each side and "along" each of the four sides of the first region

four discrete marks or "targets" (Col. 3, lines 11 – 32) located within scribe lines (32) (Figure 4) at the midpoint along a scribe line for receiving a four-sided stepper shot with the scribe line at the periphery and "marks" (Col. 2, line 37) at opposing sides of the stepper shot equal in length,

wherein one alignment target is located on each of the four sides of the first region with opposing sides of the first region equal in length and at a midpoint of a side, wherein alignment targets on the first and second sides of the first region are in mirror-image positions wherein for a zero or non-defined rotational error between first and second regions of the wafer, the alignment mark has a width.

9. Regarding Claim 3, Zhou discloses, as discussed above, that an alignment target is located at each corner of the first region.

10. Regarding Claim 7, Zhou discloses (Col. 6, lines 57 – 61) that the alignment marks in sets have an alignment with respect to each other to include perpendicular, parallel or

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other combinations to include (Col. 3, lines 21 – 29) squares, rectangles, T-shape, or a cross shape.

11. Regarding Claim 21, Zhou discloses a semiconductor structure, comprising:

a semiconductor wafer (Col.3, lines 11 –12),

a plurality of four-sided integrated circuit regions, separated by scribe lines disposed on a first surface of the wafer, and

at least one alignment target disposed in a scribe line (32) (Figure 4), the first scribe line being a common region between a first stepper shot and a second stepper shot,

wherein a fixed rotational error is present and the width of the alignment target is approximately equal to 0.18  $\mu\text{m}$  (Col. 5, lines 50 – 51).

### ***Claim Rejections – 35 U.S.C. 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou, and further in view of Wolf et al. ("Silicon Processing for the VLSI Era: Vol. 1" Lattice Press, Sunset Beach, CA., (1986), p. 478) and Banks ("Introduction to Microengineering," Demon Co., England (1999), p.2).

14. Regarding Claims 4 and 5, Zhou does not disclose the formation of targets by either a positive or negative resist process. However, the formation of features on a material (such as chrome) by these procedures is notoriously well known in the art. Wolf et al. discloses (page 478, Figure 21) the formation of "clear-field" (positive) and "dark-field" (negative) patterns, corresponding to transparent or opaque fields (raised or depressed features). Banks discloses (page 2, 3<sup>rd</sup> through 5<sup>th</sup> paragraph) how a negative image (depression on mask) is transferred through the process to a target to produce a positive feature or a negative feature. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to add Wolf et al. and Banks to Zhou to obtain a process for producing alignment targets by a positive or negative photoresist step onto scribe lines of a wafer surface to form raised or depressed target features.

### ***Response to Arguments***

15. Applicant's arguments in relation to claim rejections have been carefully considered but these have not been found to be persuasive. In regard to Applicant's argument (page 5, Response) that there is no indication of an alignment target in multiple scribe lines, Examiner does not agree. Although Zhou describes a single alignment, Applicant is reminded that an integrated circuit is present with repetitive structure on the wafer, identical to the disclosure by Applicant in Figure 8 of the instant application.

Remarks by Applicant (p.5, first par.) that the first region is disclosed in the Specification to

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"contain one or more integrated circuits" is incorrect. Rather, it is a "stepper shot" that may be comprised of multiple integrated circuit dies or a single die (Specification, p. 3, lines 9 and 10). There is no equivalence established between a "first region" and a "stepper shot," either in the Specification or in the Claim language.

Additional commentary in the Response is not germane due to the rejection of limitations in Claims 1 and 21 under 35 U.S.C. 112.

### ***Conclusions***

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(703) 308-1690**. The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Thomas Magee  
October 26, 2004



**EDDIE LEE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**

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